Docket No. 030712-21 Serial No. 10/760,359 Page 7

REMARKS

The Office Action of June 16, 2005, has been received and its contents carefully noted. By way of the present response, claims 1 and 2 are amended, and claims 11-20 are added. Claims 1-20 currently are pending.

Support for the amendments are provided in at least Figures 1 and 2 and related text of the specification. No new matter has been added. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

Claims 1-10 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Goto¹. Applicants respectfully traverse this rejection for at least the following reasons:

Each of amended independent claims 1 and 2 recite, among other things, the features of a first semiconductor chip having a central circuit area at which a high noise resistivity circuit is formed, a peripheral circuit area surrounding the central circuit area, and a low noise resistivity circuit being formed on the peripheral circuit area. Because the low noise resistivity circuit (i.e., a circuit easily subject to the influence of noise) is formed on the peripheral circuit area, influence of noise generated from wires on the first semiconductor chip is substantially reduced. Thus, the present invention facilitates remarkable improvements in the reliability of a semiconductor device in which first and second semiconductor chips are mounted. (See, for example, page 3, line 15 to page 4, line 4.)

In contrast, the Goto '662 publication does not describe the claimed combination of features including a first semiconductor chip having a central circuit area at which a high noise resistivity circuit is formed, a peripheral circuit area surrounding the central circuit area, and a low noise resistivity circuit being formed on the peripheral circuit area. Rather, Goto '662 discloses, at lines 8-10 of paragraph 0017 and lines 5-8 of paragraph 0022, that no transistors are formed in a central in a central area of the semiconductor chip (i.e., chip 103). Accordingly, the Goto '662 publication does not describe all the features recited in amended claims 1 and 2.

Accordingly, Applicants respectfully submit that the rejection is rendered moot and

The Office Action, at lines 1-2 of section 2 on page 2, circs "Goto (US2004/0018661)," but this publication number does not correspond to U.S. Patent Application Publication No. US2004/0018662 to Goto (hereinafter, "Goto '662") supplied with the Action. Additionally, the reference numbers described in connection with the cited Goto reference do not appear to correspond to the cited figures of Goto discussed in the Office Action. However, Figure 4 of Goto '662 does appear to correspond to the (Footnets continued on next page)

Docket No. 030712-21 Serial No. 10/760,359 Page 8

obviated in view of the amendments.

It is respectfully submitted that newly added claim 10 recites a similar distinction not described in the Goto '662 publication. For instance, claim 10 recites inter alia "a first semiconductor chip having a central circuit area on which a high noise resistivity circuit is formed, a peripheral circuit area surrounding the central circuit area, on which a low noise resistivity circuit is formed" As pointed out above, the Goto '662 publication explicitly discloses that no transistors are formed in a substrate area 111 of a semiconductor chip 103. Thus, Goto '662 does not describe a first semiconductor chip having a central circuit area on which a high noise resistivity circuit is formed in the context of the other recited features of claim 10. Accordingly, claim 10 is considered allowable.

The remaining claims depend from one of independent claims 1, 2 and 10, and are therefore considered allowable at least for the above reasons, and further for the additional features recited.

Additionally, Applicants submit herewith copies of a Notice of Recordation of Assignment Document dated November 2, 2002, an assignment document executed on August 16, 2001, and an assignment cover sheet (Form PTO-1619A) for U.S. Patent Application No. 09/939,801, which is the parent of U.S. Patent Application No. 10/619,003 (published as the Goto '662 application publication). As evinced by these papers, the entire title, right and interest in U.S. Patent Application No. 09/939,801, was transferred to Oki Electric Industry Co., Inc. on August 16, 2001. Also, Applicants submit that Oki Electric Industry Co., Inc. owned the subject matter of U.S. Application No. 09/939,801, and hence also the subject matter of U.S. Patent Application No. 10/619,003, and the claimed invention at the time the present application was filed. Thus, the Goto '662 publication is removed as an available reference under 35 U.S.C. §103 in connection with this application.

⁽Footnote continued from previous page)

Examiner's description in section 2. Thus, it is believed that the Examiner intended to cite the Goto *662 publication, and Figure 4 thereof, in the grounds and statements of the rejection.

Docket No. 030712-21 Serial No. 10/760,359

Page 9

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise which could be eliminated through discussions with Applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Respectfully submitted,

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